Notice of Allowability	Application No.	Applicant(s)	
	10/674,404	HOSONO ET AL.	
	Examiner	Art Unit	
	Tuan T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Preliminary Amendment filed on 12/05/2003*.

2. ☒ The allowed claim(s) is/are *2-46*.

3. ☒ The drawings filed on *01 October 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *09/985,017* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/01/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Attachment A: Search History*.

3/22/04

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

1. Claim 1 has been canceled.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 10/01/03 was filed same with the mailing date of the present application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

4. Claims 2-46 are allowed.

5. The following is an examiner's statement of reasons for allowance:

The prior art of record fail to disclose a semiconductor memory device comprising, in combination with other cited limitations, a first circuit configured to generate a first current varying in proportion to " 1.' or ,'0" of binary logic data of one end of said plurality of latch circuits; a second circuit configured to generate a second current which is preset; and a third circuit configured to compare the first current with the second current; wherein the value of " 1.. or "0" of binary logic data of said one end of said plurality of latch circuits is detected based on a result of the comparison between the first current and the second current as recited in claims 2-10.

The prior art of record fail to disclose a semiconductor memory device comprising, in combination with other cited limitations, a first circuit configured to generate a first current varying in proportion to "1" or .'0" of binary logic data of one end of said plurality of latch circuits; a second circuit is configured to generate a second current which is preset; and a third circuit configured to compare the first current with the second current; wherein the value of "1" or "0" of binary logic data of said one end of said plurality of latch circuits is detected based on a result of the comparison between the first current and the second current as recited in claims 11-18.

The prior art of record fail to disclose a semiconductor memory device comprising, in combination with other cited limitations, a first circuit configured to cause a current to flow through a current path connected to a corresponding latch circuit group of the plurality of the latch circuit groups when binary logic data of one end of said plurality of latch circuit groups is "0" and interrupt the current when the binary logic data is "1" said first circuit outputting a first current which is a sum of currents flowing through the current path; a second circuit configured to generate a second current which is preset; and a third circuit configured to compare the first current output from the first circuit with the second current output from the second circuit, said third circuit detecting the value of "1" or "0" of binary logic data of said one end of the plurality of latch circuit groups based on a result of the comparison between the first current and the second current as recited in claims 19-32.

The prior art of record fail to disclose a semiconductor memory device comprising, in combination with other cited limitations, a first circuit configured to cause a current to flow through a current path connected to a corresponding latch circuit of the plurality of the latch

circuits when binary logic data of one end of said plurality of latch circuits is "0" and interrupt the current when the binary logic data is "1" said first circuit outputting a first current which is a sum of currents flowing through the current path; a second circuit configured to generate a second current which is predetermined; a current control circuit connected to the first and second circuits, and configured to determine absolute values of the first current and the second current; and a third circuit configured to compare the first current output from the first circuit with the second current output from the second circuit, said third circuit detecting the value of "1" or "0" of the binary logic data of said one end of the plurality of latch circuits based on a result of the comparison between the first current and the second current as recited in claims 33-35, and 44.

The prior art of record fail to disclose a semiconductor memory device comprising, in combination with other cited limitations, a first circuit configured to cause a current to flow through a current path connected to a corresponding latch circuit of the plurality of the latch circuits when binary logic data of one end of said plurality of latch circuits is "0" and interrupt the current when the binary logic data is "1" said first circuit outputting a first current which is a sum of currents flowing through the current path; a second circuit configured to generate a second current which is predetermined; a current control circuit connected to the first and second circuits, and configured to determine absolute values of the first current and the second current; and a third circuit configured to compare the first current output from the first circuit with the second current output from the second circuit, said third circuit detecting the value of "1" or "0" of the binary logic data of said one end of the plurality of latch circuits based on a result of the comparison between the first current and the second current as recited in claims 36-38 and 45.

The prior art of record fail to disclose a semiconductor memory device comprising, in combination with other cited limitations, a first circuit configured to cause a current to flow through a current path connected to a corresponding latch circuit group of the plurality of the latch circuit groups when binary logic data of one end of said plurality of latch circuit groups is "0" and interrupt the current when the binary logic data is "1" said first circuit outputting a first current which is a sum of currents flowing through the current path; a second circuit configured to generate a second current which is predetermined; a current control circuit connected to the first and second circuits, and configured to determine absolute values of the first current and the second current; and a third circuit configured to compare the first current output from the first circuit with the second current output from the second circuit, said third circuit detecting the value of "1" or "0" of the binary logic data of said one end of the plurality of latch circuit groups based on a result of the comparison between the first current and the second current as recited in claims 39-43 and 46.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Nguyen whose telephone number is (571) 272-1880. The examiner can normally be reached on Mon-Thu-Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Nguyen
March 21, 2004